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Terms	Documents
L8 and L1	24

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L9

Refine Search

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Search History

DATE: Thursday, July 08, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT,USOC,EPAB,JPAB; PLUR=YES; OP=OR		
L9	L8 and l1	24	L9
L8	L7 same address same memory	77693	L8
L7	register or storage	1600045	L7
L6	L1 and l5	19	L6
L5	memory adj1 address	38785	L5
L4	(4471472| 4573146| 4601019| 5257229| 5270974| 5299164| 5303192| 5307316| 5353253| 5355340| 5377146| 5381370| 5396124| 5430679| 5446693| 5528539| 5537665)![pn]	17	L4
L3	L1 same cell	14	L3
L2	L1 same (row or column)	10	L2
L1	redundant near2 plane	159	L1

END OF SEARCH HISTORY

L9: Entry 3 of 24 File: USPT May 6, 2003

DOCUMENT-IDENTIFIER: US 6560728 B2
TITLE: Layout for semiconductor memory device having a plurality of rows and columns of circuit cells divided into first and second planes that are not simultaneously active

Brief Summary Text (14):
An additional problem with reducing the number of redundant memory elements relates to dividing the primary memory array into sub-arrays. Current memory devices divide the primary array of memory cells into sub-arrays so that only a portion of the memory need be energized in a given access, resulting in significant power reduction. Each sub-array requires its own redundant rows and columns. By dividing the memory array into two sub-arrays or "planes," the redundant rows and columns in the first plane can be substituted for any defective row or column in the primary rows/columns of memory cells in the first plane. Although the memory array could be further divided into a greater number of planes (e.g., four) to further reduce power consumption, then an even fewer number of redundant rows and columns can be employed to replace defective rows and columns in one-fourth of the primary memory array. If a greater number of errors occurred within one quarter of the memory array, then an insufficient number of redundant rows/columns will be available to compensate for such defects. Alternatively, no planes could be employed so that all of the redundant rows and columns can be used to replace defective rows and columns throughout the memory anywhere throughout the memory array. However, such a scheme requires a greater number of routing lines as compared to dividing the array into two planes.

Detailed Description Text (15):
While being spatially divided between various blocks, groups and sub-arrays of memory cells within the memory array 102, each of the redundant rows and columns are logically contiguous. For example, each of the eight redundant columns from plane A physically extends through the blocks of memory cells 219, 220, 223, 224, 227, 228, 231, 232, 235, 236, 239, 240, 243, 244, 247 and 248, or through the blocks of memory cells 203, 204, 207, 208, 211, 212, 215, 216, 251, 252, 255, 256, 259, 260, 263 and 264, all of which are in plane A. The rows and columns of redundant cells 107 and 108 in plane A do not extend through the blocks of memory cells within the plane B. Likewise, a logically contiguous row or column of redundant cells 107 or 108 in plane B physically extends through all blocks of memory cells in plane B, but none of the memory cells in plane A.

Detailed Description Text (20):
Only eight lines 138 are employed to couple the compare circuits 146 with all of the redundant rows and columns 107 and 108 in the memory array 102. By dividing the planes along boundaries defined by the shared sense amplifiers 114, no two redundant columns on either side of the shared sense amplifier will be simultaneously activated. In other words, no redundant columns 108 from plane B will be activated when redundant columns 108 from plane A are energized. Therefore, eight lines 138 can be coupled to eight redundant columns 108 running through the memory array 102, where the redundant columns can be conceptualized as having twice the length of standard columns in the array. The sense amplifiers 114 selectively enable only half of the eight redundant columns at any one time. As a result, the eight redundant columns 107 are partitioned into two sets of eight columns each

having standard length, thereby providing eight redundant columns for plane A and eight redundant columns for plane B. Otherwise, as is currently performed in the art, at least 16 lines must be routed from the compare circuits 146 to 16 separate redundant rows and columns.

Detailed Description Text (41):
Since the device 100 provides a beneficial architecture for realizing improved die area, which can allow for enhanced or improved performance of the device, systems employing the device can benefit from the present invention. Referring to FIG. 7, a block diagram of a computer system 50 that uses one or more memory devices 100 is shown. The computer system 50 includes a processor 52 for performing computer functions, such as executing software to perform desired calculations and tasks. The processor 52 is connected to the one or more memory devices 100 through a memory controller 62 that provides the appropriate signals to the memory. One or more input devices 54, such as a keypad or a mouse, are coupled to the processor 50 and allow an operator (not shown) to input data thereto. One or more output devices 56 are coupled to the processor 52 to provide the operator with data generated by the processor 52. Examples of output devices 56 include a printer and a video display unit. One or more data storage devices 58 are coupled to the processor 52 to store data on or retrieve data from external storage media (not shown). Examples of storage devices 58 and corresponding storage media include drives for hard and floppy disks, tape cassettes, and compact disc read-only memories (CD-ROMs). Typically, the processor 50 generates the address signals A0-RA9, control signals such as CAS, RAS, WE, etc., and the data that is written to the memory device 100, as shown by the address, data, control, and status buses, shown in FIG. 7.

CLAIMS:

22. A semiconductor memory device coupled to first and second voltage supply terminals, comprising: a plurality of rows and columns of primary and redundant storage means for storing bits of information, the primary and redundant storage means being divided into first and second complementary blocks; a plurality of programmable storage means for storing at least one bit of information of an address of one of the plurality of rows of primary storage means and at least one bit of information of an address of one of the plurality of columns of primary storage means, each programmable storage means comprising: first and second means for storing data, each means being coupled to the first voltage supply terminal; a single shared selection means coupled to both of the first and second means for storing data for selectively providing first and second bits of information stored in the first and second means for storing data in response to a selection signal indicating which of the first and second blocks of memory cells is active; and an output means coupled to the second voltage supply terminal and the single shared selection circuit means for providing the first and second bits of information from the single shared selection means.

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L2: Entry 1 of 10 File: USPT May 6, 2003

DOCUMENT-IDENTIFIER: US 6560728 B2
TITLE: Layout for semiconductor memory device having a plurality of rows and columns of circuit cells divided into first and second planes that are not simultaneously active

Brief Summary Text (14):
An additional problem with reducing the number of redundant memory elements relates to dividing the primary memory array into sub-arrays. Current memory devices divide the primary array of memory cells into sub-arrays so that only a portion of the memory need be energized in a given access, resulting in significant power reduction. Each sub-array requires its own redundant rows and columns. By dividing the memory array into two sub-arrays or "planes," the redundant rows and columns in the first plane can be substituted for any defective row or column in the primary rows/columns of memory cells in the first plane. Although the memory array could be further divided into a greater number of planes (e.g., four) to further reduce power consumption, then an even fewer number of redundant rows and columns can be employed to replace defective rows and columns in one-fourth of the primary memory array. If a greater number of errors occurred within one quarter of the memory array, then an insufficient number of redundant rows/columns will be available to compensate for such defects. Alternatively, no planes could be employed so that all of the redundant rows and columns can be used to replace defective rows and columns throughout the memory anywhere throughout the memory array. However, such a scheme requires a greater number of routing lines as compared to dividing the array into two planes.

Detailed Description Text (15):
While being spatially divided between various blocks, groups and sub-arrays of memory cells within the memory array 102, each of the redundant rows and columns are logically contiguous. For example, each of the eight redundant columns from plane A physically extends through the blocks of memory cells 219, 220, 223, 224, 227, 228, 231, 232, 235, 236, 239, 240, 243, 244, 247 and 248, or through the blocks of memory cells 203, 204, 207, 208, 211, 212, 215, 216, 251, 252, 255, 256, 259, 260, 263 and 264, all of which are in plane A. The rows and columns of redundant cells 107 and 108 in plane A do not extend through the blocks of memory cells within the plane B. Likewise, a logically contiguous row or column of redundant cells 107 or 108 in plane B physically extends through all blocks of memory cells in plane B, but none of the memory cells in plane A.

Detailed Description Text (20):
Only eight lines 138 are employed to couple the compare circuits 146 with all of the redundant rows and columns 107 and 108 in the memory array 102. By dividing the planes along boundaries defined by the shared sense amplifiers 114, no two redundant columns on either side of the shared sense amplifier will be simultaneously activated. In other words, no redundant columns 108 from plane B will be activated when redundant columns 108 from plane A are energized. Therefore, eight lines 138 can be coupled to eight redundant columns 108 running through the memory array 102, where the redundant columns can be conceptualized as having twice the length of standard columns in the array. The sense amplifiers 114 selectively enable only half of the eight redundant columns at any one time. As a result, the eight redundant columns 107 are partitioned into two sets of eight columns each

having standard length, thereby providing eight redundant columns for plane A and eight redundant columns for plane B. Otherwise, as is currently performed in the art, at least 16 lines must be routed from the compare circuits 146 to 16 separate redundant rows and columns.

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L9: Entry 15 of 24 File: USPT Jan 6, 1998

DOCUMENT-IDENTIFIER: US 5706292 A
TITLE: Layout for a semiconductor memory device having redundant elements

Brief Summary Text (14):
An additional problem with reducing the number of redundant memory elements relates to dividing the primary memory array into sub-arrays. Current memory devices divide the primary array of memory cells into sub-arrays so that only a portion of the memory need be energized in a given access, resulting in significant power reduction. Each sub-array requires its own redundant rows and columns. By dividing the memory array into two sub-arrays or "planes," the redundant rows and columns in the first plane can be substituted for any defective row or column in the primary rows/columns of memory cells in the first plane. Although the memory array could be further divided into a greater number of planes (e.g., four) to further reduce power consumption, then an even fewer number of redundant rows and columns can be employed to replace defective rows and columns in one-fourth of the primary memory array. If a greater number of errors occurred within one quarter of the memory array, then an insufficient number of redundant rows/columns will be available to compensate for such defects. Alternatively, no planes could be employed so that all of the redundant rows and columns can be used to replace defective rows and columns throughout the memory anywhere throughout the memory array. However, such a scheme requires a greater number of routing lines as compared to dividing the array into two planes.

Detailed Description Text (15):
While being spatially divided between various blocks, groups and sub-arrays of memory cells within the memory array 102, each of the redundant rows and columns are logically contiguous. For example, each of the eight redundant columns from plane A physically extends through the blocks of memory cells 219, 220, 223, 224, 227, 228, 231, 232, 235, 236, 239, 240, 243, 244, 247 and 248, or through the blocks of memory cells 203, 204, 207, 208, 211, 212, 215, 216, 251, 252, 255, 256, 259, 260, 263 and 264, all of which are in plane A. The rows and columns of redundant cells 107 and 108 in plane A do not extend through the blocks of memory cells within the plane B. Likewise, a logically contiguous row or column of redundant cells 107 or 108 in plane B physically extends through all blocks of memory cells in plane B, but none of the memory cells in plane A.

Detailed Description Text (20):
Only eight lines 138 are employed to couple the compare circuits 146 with all of the redundant rows and columns 107 and 108 in the memory array 102. By dividing the planes along boundaries defined by the shared sense amplifiers 114, no two redundant columns on either side of the shared sense amplifier will be simultaneously activated. In other words, no redundant columns 108 from plane B will be activated when redundant columns 108 from plane A are energized. Therefore, eight lines 138 can be coupled to eight redundant columns 108 running through the memory array 102, where the redundant columns can be conceptualized as having twice the length of standard columns in the array. The sense amplifiers 114 selectively enable only half of the eight redundant columns at any one time. As a result, the eight redundant columns 107 are partitioned into two sets of eight columns each having standard length, thereby providing eight redundant columns for plane A and eight redundant columns for plane B. Otherwise, as is currently performed in the

art, at least 16 lines must be routed from the compare circuits 146 to 16 separate redundant rows and columns.

Detailed Description Text (41):
Since the device 100 provides a beneficial architecture for realizing improved die area, which can allow for enhanced or improved performance of the device, systems employing the device can benefit from the present invention. Referring to FIG. 7, a block diagram of a computer system 50 that uses one or more memory devices 100 is shown. The computer system 50 includes a processor 52 for performing computer functions, such as executing software to perform desired calculations and tasks. The processor 52 is connected to the one or more memory devices 100 through a memory controller 62 that provides the appropriate signals to the memory. One or more input devices 54, such as a keypad or a mouse, are coupled to the processor 50 and allow an operator (not shown) to input data thereto. One or more output devices 56 are coupled to the processor 52 to provide the operator with data generated by the processor 52. Examples of output devices 56 include a printer and a video display unit. One or more data storage devices 58 are coupled to the processor 52 to store data on or retrieve data from external storage media (not shown). Examples of storage devices 58 and corresponding storage media include drives for hard and floppy disks, tape cassettes, and compact disc read-only memories (CD-ROMs). Typically, the processor 50 generates the address signals A0-RA9, control signals such as CAS, RAS, WE, etc., and the data that is written to the memory device 100, as shown by the address, data, control, and status buses, shown in FIG. 7.

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L9: Entry 17 of 24 File: USPT Nov 19, 1996

DOCUMENT-IDENTIFIER: US 5577055 A
TITLE: Method and circuit device to control a memory

Abstract Text (1):
A method and a circuit device control insertion and storage of digital information in a memory and retrieval of the information from the memory. The method and circuit device ensure the digital information is correctly read out of the memory in the form of a number of coordinated bit positions, and the digital information is used to control one or several functions. The information intended to be inserted into the memory is given an address belonging to the memory. First control-sum-carrying bit positions are calculated from the bit positions of the digital information and their values coming into the memory according to a selected evaluation function. The bit positions of the digital information are stored in an address within the memory, and the first control-sum-carrying bit positions are stored in an address within a control memory. Second control-sum-carrying bit positions are calculated when the bit positions of the digital information stored in the address in the memory are read out according to the selected evaluation function. The bit positions of the read information, and their values, are accepted as correct, and a circuit is activated through a signal on a conductor, if a following comparison between the first and second control-sum-carrying bit positions shows that they are identical.

Brief Summary Text (11):
A parity control and a device for a chip-related memory are previously known through the European patent publication EP A2 0 449 052 which describes a parity control of address signals. The parity is controlled before a digitized word is stored within a memory. An integrated circuit with an input register to receive a number of addressing bits, a set of memories to store information in a number of addressable storage positions, a control unit to evaluate at least one of the addressable storage positions corresponding to the address bits and a unit to control the parity of the address bits. A memory circuit controls parity control before a digitized word is stored in the memory circuit.

Brief Summary Text (16):
IBM Technical Disclosure Bulletin, vol. 24, no. 1B, p. 794 (June 1981), describes a method of ensuring that information stored within a memory is correctly readable. A parity bit, belonging to a data byte, is generated for every data byte or word comprising a number of bit positions. The value of a parity bit is determined by the number of bits with the value "1" in both the data word and the addressing value in the address register of the memory. A further parity bit is generated at the readout of the data word from the memory, and this is calculated taking the number of 1-bit positions or the number of 1-bits in both the data word and the address initiating the readout into consideration. This further parity bit is thereafter compared with the previously stored parity bit and an error signal is generated if there is a difference.

Brief Summary Text (17):
U.S. Pat. No. 4,809,278 describes a system for ensuring that information stored in a memory is correctly readable. Parity bits are generated for every word that is stored in an addressed position. The number of parity bits can be selected to be

the same as the number of input connections of each storage chip used in the storage structure. A first and a second set of Exclusive-Or gates generate a first and second set of parity data for every read-write cycle addressing the same memory position. A help-memory for parity bits receives the first set of parity data for storage in positions corresponding to similar positions in each memory chip so that the same address data will read the first set of bits of parity data corresponding to each address in the structured memory. These parity data are the input signals to a second set of Exclusive-Or gates intended to form a second set.

Brief Summary Text (19):
European patent publication EP A1 463 210 describes a circuit intended to control the storage in and addressing of a memory. At least one write address register and at least one read address register are used. Every one of the check bits of the data word is Exclusive-Or-related with a bit in the address position. The check bits are Exclusive-Or-related with the bits of the address position once again at the readout of the word in order to regenerate their original values, so that the parity of the data word can be controlled.

Brief Summary Text (26):
A control memory should comprise a register or a FIFO memory in which selected information regarding respective digital information, structured into a data packet or a data cell, can be stored. The selected information should comprise at least the first control-sum-carrying positions and/or the address of the data packet and/or position in the memory. Information regarding the classification and/or order of priority within a selected category of respective data packet should be stored in the register or control memory. Information or a data packet, within a certain category, should be read out in turn (FIFO) through an adapted readout circuit.

Brief Summary Text (34):
The present invention further provides a control memory comprising a register in which selected information regarding respective data packet, such as the first control-sum-carrying bit positions and the address of the data packet and/or position in the main memory, is stored. Information regarding the classification of respective data packet is also stored in the control memory. Information or a data packet, within a certain category, is read out in turn through a readout circuit. If there is an agreement between the first, read from the control memory, and second, calculated, control-sum-carrying bit positions, but there is a lack of agreement between further bit positions, belonging to the data packet, the read information or data packet is still accepted as correct.

Detailed Description Text (4):
The transmitter 3 coacts, through a line or connection 4, with a line-related receiver unit 5 which is, through a line or connection 6, connected to an input circuit 7. The input circuit 7 is, in turn, through a line or connection 8, in coaction with a number of connecting terminals 9, belonging to an ATM-selector 10. The ATM-selector 10 is equipped with two redundant connecting planes or connecting cores 11, 12 which, through circuits not illustrated, coact with the signal receiving unit 3a and the terminal 2. The lines 4, 6 and 8 can be made out of one or several physical connections or conductors.

Detailed Description Text (33):
In a second embodiment, with data cells comprising control-sum-carrying bit positions according to FIG. 4, the unit 53c can be arranged to read the control-sum-carrying bit positions 220c and/or the bit positions 200c, or alternatively only the bit positions 200c or the bit positions 200c'. An incoming data cell 200 will thus be completely stored in a last memory position 51a'. At the same time control-sum-carrying bit positions, such as a check sum, that have been pointed out and read, are stored only in the register 55 at a corresponding address position. As the pointer in the memory 51 is moved, the pointer in the memory or register 55

is moved in the same way in order to keep the positions corresponding to each other.

Detailed Description Text (34):
The embodiment according to FIG. 6 is intended to illustrate a position where the complete data cell 200 is read out 200' of the memory 51 from the position 51a and stored in the storage circuit 61 at the same time a corresponding check sum 220c" is read out of the corresponding address position in the register 55. An address position in the control memory 55 is activated, and the control unit 56 will receive information regarding the value of the control-sum-carrying bit positions 220c', according to a selected calculation in the unit 62. A control-sum 220c" is stored in the register 55 when a control unit 56, through a unit 66 and a conductor 58, requires a readout of a data cell from the main memory 51.

Detailed Description Text (37):
The embodiment described with reference to FIG. 7 can be regarded as a development of the embodiment according to FIG. 6. FIG. 7 is intended to illustrate a number of FIFO memories serving as main memories 51, 751a, 751b, 751c oriented in "parallel" to each other, each intended to store data cells of one and the same category. A corresponding number of registers or control memories 55, 755a, 755b, 755c are for these purposes required, each given its own category. The main memory 51 corresponds to the register or control memory 55, the memory 751a corresponds to the register 755a and so forth, whereby corresponding memories and registers are stepped synchronously, always pointing at the same address position.

Detailed Description Text (40):
An embodiment according to FIG. 8 is illustrated in order to get a better used memory capacity and in order to be able to store data cells of the same or different categories more efficiently. The embodiment according to FIG. 8 requires a main memory 51 of a more complex nature since the position of a respective data cell is unanimously determined, and a data cell can be given any available position. The main memory 51 and register 55 can be "virtual" FIFO memories or buffer circuits. In this case, selected information intended for each data cell, such as the first control-sum-carrying bit positions 220c and the selected address 51a and/or position of the data packet, is stored in a register 55 serving as a control memory. The register is, besides this, able to store information regarding the category of a respective data packet.

Detailed Description Text (42):
The memory 51 in FIG. 8 provides a storage of the data cell within any number of addresses, and means are therefore required to determine what address positions that are available. These available address positions are sorted into a so called "available list".

Detailed Description Text (50):
The field 220c' is calculated whenever a data cell is read out of the buffer memory 51. The result from this calculation is compared with both the field 220c, which actually was a part of the cell, and with the field that was stored in the queue with the pointer within the register 55. It is assumed that the data cell is correct or correctly read out if the newly calculated field 220c' is identical with the one that already was in the data cell and that the logic has had a proper function with the least significant address bits, those used at the addressing within the data cell. If, besides this, the newly calculated field 220c' is identical with the field that is stored in the queue together with the pointer within the register 55, it is obvious that the right data cell really has been read out, meaning that the logic and the most significant address bits, those used for the addressing, have had a proper function and that the pointer really pointed out in the right way.

CLAIMS:

11. The method of claim 1, wherein the control memory comprises a register in which selected information regarding a respective data packet, such as the first calculated control-sum-carrying bit positions and the address of the dam packet and/or position in the main memory, is stored, and information regarding the classification of the respective data packet is stored.

23. The device of claim 14, wherein the control memory comprises a register in which selected information regarding a respective data packet, such as the calculated first control-sum-carrying bit positions and the address of the data packet and/or position in the main memory, is stored.

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L9: Entry 20 of 24 File: USPT Oct 10, 1995

DOCUMENT-IDENTIFIER: US 5457789 A
TITLE: Method and apparatus for performing memory protection operations in a single instruction multiple data system

Detailed Description Text (21):
In FIG. 3 an exemplary permission table is shown. The table is organized such that the rows correspond to respectively different section of memory and the columns correspond to respectively different parameters of a process. In the exemplary embodiments of the invention, each row may be assigned to a respectively different process or multiple rows may be grouped and the groups assigned to respectively different processes. It is understood that any scheme for determining the allowablity of a memory access may be used. In FIGS. 3, 5 and 6, the exemplary permission tables include R+1 rows, corresponding to R+1 sections of memory. In general, there may be any number of memory sections, although any number beyond the total number of memory planes is redundant.

Detailed Description Text (28):
In FIG. 5, circuitry representing a logical implementation of the permission table of FIG. 3 is shown. The optional permission bit plane circuitry is not shown in this FIGURE. The circuit of FIG. 5 compares the address of a memory access with addresses stored in the permission table. This circuit also determines whether read and write operations are allowed at a specified address. When a memory access instruction is transmitted from the instruction decoder 802 to the permission table 805, a comparator 504 determines whether the location of this memory access is greater than or equal to a bit plane which is designated in lower bound register 501. This register corresponds to the lower bound value LBR shown in FIG. 3.

Detailed Description Text (37):
In another alternative embodiment of the invention, the above schemes are modified so that the permission bit plane resides in a memory bit-plane having an address that is either a fixed value or a value designated by a register in the control unit 820. In this instance it is only necessary that the bit-plane registers 702, 704 and 706 and the permission bit-plane address bus convey a single bit of information, indicating whether the permission bit-plane should be accessed.

Detailed Description Text (38):
In yet another alternative embodiment, the first two schemes described above are modified so that the permission bit plane occupies a set of registers 808, one set per processing element. In this instance, it may be possible to read, test and act on the permission bits more quickly than if they are stored as a part of the processing element memory array 840. For this embodiment of the invention, the permission bit-plane address bus 707 conveys only a single-bit of information: whether the permission bit-plane registers 808 are to be used for the instruction.

L2: Entry 3 of 10 File: USPT Dec 19, 2000

DOCUMENT-IDENTIFIER: US 6163860 A
** See image for Certificate of Correction **
TITLE: Layout for a semiconductor memory device having redundant elements

Brief Summary Text (14):
An additional problem with reducing the number of redundant memory elements relates to dividing the primary memory array into sub-arrays. Current memory devices divide the primary array of memory cells into sub-arrays so that only a portion of the memory need be energized in a given access, resulting in significant power reduction. Each sub-array requires its own redundant rows and columns. By dividing the memory array into two sub-arrays or "planes," the redundant rows and columns in the first plane can be substituted for any defective row or column in the primary rows/columns of memory cells in the first plane. Although the memory array could be further divided into a greater number of planes (e.g., four) to further reduce power consumption, then an even fewer number of redundant rows and columns can be employed to replace defective rows and columns in one-fourth of the primary memory array. If a greater number of errors occurred within one quarter of the memory array, then an insufficient number of redundant rows/columns will be available to compensate for such defects. Alternatively, no planes could be employed so that all of the redundant rows and columns can be used to replace defective rows and columns throughout the memory anywhere throughout the memory array. However, such a scheme requires a greater number of routing lines as compared to dividing the array into two planes.

Detailed Description Text (15):
While being spatially divided between various blocks, groups and sub-arrays of memory cells within the memory array 102, each of the redundant rows and columns are logically contiguous. For example, each of the eight redundant columns from plane A physically extends through the blocks of memory cells 219, 220, 223, 224, 227, 228, 231, 232, 235, 236, 239, 240, 243, 244, 247 and 248, or through the blocks of memory cells 203, 204, 207, 208, 211, 212, 215, 216, 251, 252, 255, 256, 259, 260, 263 and 264, all of which are in plane A. The rows and columns of redundant cells 107 and 108 in plane A do not extend through the blocks of memory cells within the plane B. Likewise, a logically contiguous row or column of redundant cells 107 or 108 in plane B physically extends through all blocks of memory cells in plane B, but none of the memory cells in plane A.

Detailed Description Text (20):
Only eight lines 138 are employed to couple the compare circuits 146 with all of the redundant rows and columns 107 and 108 in the memory array 102. By dividing the planes along boundaries defined by the shared sense amplifiers 114, no two redundant columns on either side of the shared sense amplifier will be simultaneously activated. In other words, no redundant columns 108 from plane B will be activated when redundant columns 108 from plane A are energized. Therefore, eight lines 138 can be coupled to eight redundant columns 108 running through the memory array 102, where the redundant columns can be conceptualized as having twice the length of standard columns in the array. The sense amplifiers 114 selectively enable only half of the eight redundant columns at any one time. As a result, the eight redundant columns 107 are partitioned into two sets of eight columns each having standard length, thereby providing eight redundant columns for plane A and

eight redundant columns for plane B. Otherwise, as is currently performed in the art, at least 16 lines must be routed from the compare circuits 146 to 16 separate redundant rows and columns.

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L2: Entry 4 of 10 File: USPT Jan 25, 2000

DOCUMENT-IDENTIFIER: US 6018811 A

** See image for Certificate of Correction **

TITLE: Layout for semiconductor memory device wherein intercoupling lines are shared by two sets of fuse banks and two sets of redundant elements not simultaneously active

Brief Summary Text (14):

An additional problem with reducing the number of redundant memory elements relates to dividing the primary memory array into sub-arrays. Current memory devices divide the primary array of memory cells into sub-arrays so that only a portion of the memory need be energized in a given access, resulting in significant power reduction. Each sub-array requires its own redundant rows and columns. By dividing the memory array into two sub-arrays or "planes," the redundant rows and columns in the first plane can be substituted for any defective row or column in the primary rows/columns of memory cells in the first plane. Although the memory array could be further divided into a greater number of planes (e.g., four) to further reduce power consumption, then an even fewer number of redundant rows and columns can be employed to replace defective rows and columns in one-fourth of the primary memory array. If a greater number of errors occurred within one quarter of the memory array, then an insufficient number of redundant rows/columns will be available to compensate for such defects. Alternatively, no planes could be employed so that all of the redundant rows and columns can be used to replace defective rows and columns throughout the memory anywhere throughout the memory array. However, such a scheme requires a greater number of routing lines as compared to dividing the array into two planes.

Detailed Description Text (15):

While being spatially divided between various blocks, groups and sub-arrays of memory cells within the memory array 102, each of the redundant rows and columns are logically contiguous. For example, each of the eight redundant columns from plane A physically extends through the blocks of memory cells 219, 220, 223, 224, 227, 228, 231, 232, 235, 236, 239, 240, 243, 244, 247 and 248, or through the blocks of memory cells 203, 204, 207, 208, 211, 212, 215, 216, 251, 252, 255, 256, 259, 260, 263 and 264, all of which are in plane A. The rows and columns of redundant cells 107 and 108 in plane A do not extend through the blocks of memory cells within the plane B. Likewise, a logically contiguous row or column of redundant cells 107 or 108 in plane B physically extends through all blocks of memory cells in plane B, but none of the memory cells in plane A.

Detailed Description Text (20):

Only eight lines 138 are employed to couple the compare circuits 146 with all of the redundant rows and columns 107 and 108 in the memory array 102. By dividing the planes along boundaries defined by the shared sense amplifiers 114, no two redundant columns on either side of the shared sense amplifier will be simultaneously activated. In other words, no redundant columns 108 from plane B will be activated when redundant columns 108 from plane A are energized. Therefore, eight lines 138 can be coupled to eight redundant columns 108 running through the memory array 102, where the redundant columns can be conceptualized as having twice the length of standard columns in the array. The sense amplifiers 114 selectively enable only half of the eight redundant columns at any one time. As a result, the

eight redundant columns 107 are partitioned into two sets of eight columns each having standard length, thereby providing eight redundant columns for plane A and eight redundant columns for plane B. Otherwise, as is currently performed in the art, at least 16 lines must be routed from the compare circuits 146 to 16 separate redundant rows and columns.

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